Belgacem Ben Hedia

PhD-Engineer in Embedded & Real-Time System

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Skills

Embedded **software architecture** exploration; **Distributed** systems; IoT; Real-time system **design methodology**; **Formal** V&V and design; **Software design** expertise; **RTOS**; Source-code construction and optimization; **Teaching/learning** & undergraduate/courses management; **Establishment/management** of collaborative research projects; **Supervision** of PhD/MSc students; Management of **research team**; **Scientific events** organisation and management; IT infrastructure administration/management.

Research fields (more details on page 6)

Embedded & real-time system design; Software architecture exploration and optimization; Real-time properties verification and validation (V&V); Real-time & embedded operating systems; Code generation from high level design languages and tools.

Teaching (more details on page 4)

Lecture courses *Engineer, Engineer by apprenticeship.*
Embedded and real-time system design (BSc/MSc/Engineer degree); Software engineering (Engineer degree); Introduction to database (BSc degree); Object-oriented programming (BSc degree).

Practical courses *Engineer, Engineer by apprenticeship.*
Introduction to real-time systems (BSc degree); Design and integration of a real-time industrial application (BSc degree); Embedded and real-time system implementation in transversal project (Engineer degree); Advanced operating system - RTOS (BSc degree); Introduction to UNIX operating system (BSc degree).

Publications, Tools & Research community activities

Publications (more details on page 8) .
13 international conferences & workshops, 1 french journal, 4 french conferences & workshop, 2 proceedins editor, PhD thesis

Conferences/Scientific events .
Program co-chair: VECoS'2016, VECoS'2015, ISDA'2014
Editor: IJCCBS special issue
General co-chair: CPS Summer School'2016, RTNS'2014, JED'2008
Program commitee/Reviewer: VECoS'[2012..2016], EWiLi'14, ISDA'2014, JRWRTC'2007
Scientific seminars organizer: TLA+ (Leslie Lamport), BIP (Verimag), Safety (Airbus aerospace), Model transformation (UBO)
Advisory board member: Mathworks (code generarion)

PhD/Master student advising (more details on page 6) .
2 PhD thesis (finishing), 1 PhD thesis (starting), 3 MSc thesis (defended)

Tools .
QuaRTOS, C2TLA+, TT-BIP code genrator, Design space exploration tool

Employment

Aug. 2010 – to present
Researcher-Engineer (Expert in real-time systems) *CEA LIST*, Saclay, France.
Research work on embedded and real-time software architecture exploration and correct-by-design application construction. This work forms part of several collaboratives projects (industrial and academics partners) aimed at generating a correct-by-design executable code from high level models (typ. Modelica, BIP: a component based approach,...)

- *From high-level models to optimized real-time executable code on a Time-Triggered RTOS (European collaborative project, 2 PhD students).*
- *Embedded code source analysis and verification: model-checking (TLA+), Proof and static analysis (french national collaborative project, PhD students, industrial collaborative project).*
- *Benchmark and evaluation of several RTOS: decision tool (QuRTOS) to evaluate/explore the adequacy between an embedded real-time application and a most suitable RTOS (internal project, MsC student)*
- *IT infrastructure administrator/manager: responsible of the IT asset management, IT infrastructure, tuleap (software forge) server administrator, equipment selection and purchase (computers, servers, embedded bords, licenses), users accounts management and enforcement of ASSI (security) of my lab*

May 2009 – Jul. 2010
Researcher *Procton Labs*, Guyancourt, France.
Research work on a framework allowing the construction and execution of application on a distributed and heterogeneous architecture.

- *The design and specification of the virtualization of distributed objects referencing system in the framework level.*
- *The design and specification of the distributed virtual processes and threads, and data sharing.*

Sep. 2007 – Apr. 2009
Assistant Professor *ESISAR-INPG / INSA-Lyon*, Valances / Lyon, France.
Teaching and research work on embedded and real-time systems.

- *Teaching several lectures and practical courses in the topics of: embedded and real-time system design; software engineering; operating system & RTOS, Object-oriented programming, database and UNIX operating system and shell. These courses was taught for various degree (BSc/MSc/Engineer degree) normal and by apprenticeship.*
- *Research on modelling and verification of device driver using formal synchronous methods and language.*

Feb. 2005 – Dec. 2008
PhD Thesis *CITI Laboratory - INSA Lyon*, Lyon, France.
Research work on timing analysis of data acquisition system: approach based on timed automata and observer.

- *Model-checking, timed-automata, control application, device driver, formal modelling, end-to-end delay analysis, QoS, observer, temporal logics.*

Feb. 2004 – Jul. 2004
Master Degree Thesis *INSA Lyon*, Lyon, France.
Formal modelling and QoS evaluation of embedded real-time device driver

Feb. 2003 – Jul. 2003
Engineering Diploma Project *INSA Lyon*, Lyon, France.
A methodology for modelling hardware architectures using UML

Education

2008 **PhD** *Computer sciences: Embedded & real-time system* *INSA Lyon*, Lyon, France.

2004 **MSc** *Computer sciences: Communicating Systems* *INSA Lyon*, Lyon, France.

2003 **Diploma of Engineering** *Computer sciences: Embedded & real-time system* *Faculty of Sciences of Tunis*, Tunis, Tunisia.

Technical Skills

Languages:	C/C++, Python, Java, JavaScript, PHP, XHTML, CSS, Latex, Modelica	OS/RTOS:	Linux/Windows, VxWorks, FreeRTOS, μC/OSII
Tools/IDE:	Cross-Compilation (gcc, gdb, make), script bash/sed/awk, svn/git, Eclipse, NetBeans	Soft./Others:	OpenModelica, MATLAB, BIP, Fractal(Mind), Word/Excel/PowerPoint, Tuleap, Apache, MySQL, CMS, Wiki

Languages

French & Arabic	**Native/Bilingual**	English	**Professional/Fluent**

Teaching details (non-exhaustive list)

Title: ***Introduction safety and security***

Degree: 3ed year of french engineering school - CNAM (computer engineering)

Objectives: Introduction to the notion of safety and security

Description: This course aims to introduce the notion of safety and security in critical systems. After an introduction of largest known bugs in critical systems, and the need for security and safety. The course is organized in two steps, the first step detail the major outlines of safety strategies. the second steps of the course is rather interested to specified security problem (security strategy, access right, cryptography...)

Title: ***Introduction to embedded system***

Degree: 3ed year of french engineering school - CPE Lyon (computer engineering)

Objectives: Introduction to specification and implementation of embedded software

Description: This practical course provides an overview of the various steps of the embedded systems design and details the used hardware architecture and RTOS. One focus is given on the specific aspects of operating systems for embedded systems. At the end of this course, the student are able to implement a basic embedded application (in C language) using services provided by embedded operating systems (in particular, μ C / OS II) particularly the scheduling, tasks, messages boxes, semaphores.

Title: ***Design of real-time systems***

Degree: 4th & 5th year of french engineering school - INSA Lyon & ESISAR INPG (computer engineering)

Objectives: This module (lectures & tutorials) aims at design a real-time application such as a vending machine.

Description: After an introduction to real-time systems, a specification languages for real-time systems is detailed. In tutorials, students design a control application of the vending machine using an MDE formalism, a focus is given on the hierarchical design through several specification levels.

Title: ***Design and integration of industrial real-time systems***

Degree: 4th year of french engineering school - INSA Lyon (computer engineering)

Objectives: This practical project follows the work of students on advanced operating systems, the goal here is to make them aware of the peculiarities of embedded systems.

Description: As they were brought into an other course to studies timing constraints in the implementation of systems, the goal here is to make them aware of the specificities of an embedded systems and questions that arise when one splint to specification and design of such systems. The student implement the description of an adjustable seat controller. Using MDE notation, it should start from the needs and specify different controller functionality (adjustable, heating, maintenance...)

Title: ***Real-time and embedded system***

Degree: 5th year of french engineering school - INSA Lyon (transversal: computer/electrical/telecommunication engineering)

Objectives: This transversal module (lectures, tutorials & practical courses) aims at design a real-time and embedded system for students from three departments (computer science, electrical and telecommunication engineering).

Description: The module is organized around a common theme project (car radio application on MSP430 bords with μC/OSII RTOS) and a series of advanced courses taught by teachers from different departments. This organization allows students to give each department a bag on the issues addressed in other departments and show them how their skills are complementary and can be articulated in a project around embedded systems

Title: ***Advanced operating system (the real-time operating systems)***

Degree: 4th year of french engineering school - INSA Lyon (computer engineering)

Objectives: This practical courses is designed to show students the particular constraints associated with the development using constrained operating systems (real-time).

Description: The subject of this course is the implementation of a device driver (presence sensors) into an real-time operating system typically used in embedded applications (in this case VxWorks). The use of an industrial RTOS allows students to grasp more easily the problems of the domains (including through simulation tools provided with VxWorks).

Title: ***Introduction to UNIX operating systems***

Degree: 1st year of french engineering school - ESISAR INPG (computer engineering)

Objectives: This practical course is designed to introduce the basic Unix commands and the basics of programming in a Linux environment (shell script).

Description: It is organized as a series of practical courses wherein the student discovers step by step the Unix operating system, a file management system and the main basic and advanced controls. This course introduces also the basics concepts of shell scripts.

Title: ***Object oriented programming in JAVA***

Degree: 3ed year of french engineering school - ESIAR INPG (computer engineering)

Objectives: This courses (lecture and practical) is designed to understand the principles and concepts of object oriented programming (OOP) and learn the JAVA language.

Description: This module provides an understanding of OOP and the main concepts of OOP: encapsulation, inheritance and polymorphism. But also master an object-oriented language (JAVA) and how to link different areas, typically the software engineering and OOP while trying to find a good compromise between theory and practice (JAVA).

Title: ***Software engineering***

Degree: 4ed year of french engineering school - INSA Lyon & ESISAR INPG (computer engineering)

Objectives: This lecture course aims to initiating student to software engineering (using UML).

Description: The objectives of this module is to understand the software engineering in order to capture the main steps of the software life cycle. The focus is particularly placed on the oriented objects methods in the analysis and design phases. The module allows to identify the following points: the object-oriented software development, UML modeling, design by abstraction, case study design, design patterns and software testing.

Research details

My research focuses especially on the topics of: Embedded & real-time system design; distributed systems; Software architecture exploration and optimization; Real-time properties verification and validation (V&V); Real-time & embedded operating systems; Code generation from high level design languages and tools.

PhD Thesis

Entitled *Timing analysis of data acquisition system: an approach based on timed automata and observer*. In the context of the embedded real-time systems control, my PhD aims to model and evaluate timing properties (end-to-end delays, precision ...) in the acquisition and control chain (sensor –> device driver –> control application –> device driver –> actuator). The approach is based on timed automata for system and device driver modelling, and observer for the properties (end-to-end delay precision...) evaluation.

Design space exploration & code genration

Correct implementation deriving from high level model:

In this level, we propose an automatic transformation process from compound based approach (RT-BIP) models into applications for the target platform based on a multi-scale TT approach. Execution platform model (task model) paradigms and specificities are integrated during the transformation process and have been fully implemented (TT-BIP code generator). Transformation and code generation are correct-by-design and its correctness is proved. This work was preceded by a proof of concept in OPENPROD ITEA2 project who tried to generate multi-core source code from Modelica model into TT implementation.

Design space exploration and optimization technics

In this level, we aim to propose setting-up of a catalog of strategies, rules and good practices in order to formalize and optimize the function clustering into tasks. These strategies will take into account the specificities and criticality of functions and identify the dependence and conflicts of various techniques. The obtained application architectures are evaluated and a tradeoff between several clustering schemas is given. This work is implemented in a design space exploration framework. This work is complemented by a benchmark of several RTOSs, and the implementation of QuaRTOS, a multi-criteria decision analysis platform, that helps user to to evaluate/explore the adequacy between a given application characteristics and the more adapted RTOSs

Embedded and real-time system V&V

Model cheking C code:

Verifying software systems automatically from their source code rather than modelling them in a dedicated language gives more confidence in establishing their properties. In this work we have proposed a formal specification and verification approach for concurrent C programs directly based on the semantics of C. A set of translation rules are defined and implemented in a tool (C2TLA+) that automatically translates C code into a TLA+ specification. The TLC model checker is used on this specification to generate a model, allowing to check the absence of runtime errors and dead code in the C program in a given configuration. Interactions between translated specifications and manually written ones are evaluated: check the C code against safety or liveness properties; provide concurrency primitives or model hardware that cannot be expressed in C; and use abstract versions of translated C functions to address the state explosion problem. All these verifications have been conducted on a part of the microkernel of the PharOS real-time system.

Static analysis of C code: The CHRONO project in collaboration with IRSN aims to analyze and verify statically a C code of a real-time application. Real-time functions are addressed like: semaphore, creation/destruction of tasks, timing function. In this project I have implemented a module that identify shared variables in a C code, identify semaphores that protect these shared variables, and analyze all tasks control graphs to verify whether these shared variables are correctly protected by identified semaphores.

PhD/Master advising

Briag LE NABEC (PhD) Started in October 2015, 80% of supervision, with Pr. Jean-Philippe BABAU (UBO, Lab-STIC). *"Design space optimization and exploration of real-time and embedded software architecture"*.

Hela GUSEMI (PhD) Finishing, 60% of supervision, with Dr. Simon BLIUDZE (EPFL) & Pr. Saddek BEN-SALEM (Verimag). *"Validation of real-time applications specifications: An approch based on correct-by-design real-time application construction"*.

Amira METHNI (PhD) Fnishing, 40% of supervision, with Dr. Matthieu LEMERRE (CEA LIST) & Kamel BARKAOUI (CNAM) & Serge HADDAD (LSV, ENS Cachan). *"A formal approach to design and verify critical systems"*.

Briag LE NABEC (Master) UBO, 6 months, 2015. *"Code generation for real-time embedded application from high-level modeling language"*.

Moez RABAI (Master) ENSMA, 6 months, 2012. *"Formalization of tasks structure generation strategy of an embedded real-time application: an approach based on the PHAROS execution model"*.

Publications

[1] H. Guesmi, B. Ben Hedia, S. Bliudze, M. Jan, and S. Bensalem, "Towards correct transformation: From high-level models to time-triggered implementations," in *Proc. of WiP RTAS*, 2016.

[2] B. Ben Hedia, E. Hamelin, C. Mraidha, and S. Tucci, "Model-compilation challenges [for cyber-physical systems (cps)]," in *Proc. of ERTSS*, pp. 238–248, 2016.

[3] H. Guesmi, B. Ben Hedia, S. Bliudze, S. Bensalem, and J. Combaz, "Towards time-triggered component-based system models," in *The Tenth International Conference on Software Engineering Advances (ICSEA)*, 2015.

[4] A. Methni, M. Lemerre, B. Ben Hedia, S. Haddad, and K. Barkaoui, "Verifying and constructing abstract tla specifications: Application to the verification of c programs," in *The Tenth International Conference on Software Engineering Advances (ICSEA)*, 2015.

[5] A. Methni, B. Ben Hedia, M. Lemerre, S. Haddad, and K. Barkaoui, "State space reduction strategie for model checking concurrent c programs," in *9th International Workshop on Verification and Evaluation of Computer and Communication Systems (VECoS)*, 2015.

[6] A. Methni, M. Lemerre, B. Ben Hedia, S. Haddad, and K. Barkaoui, "Specifying and verifying concurrent c programs with tla+," in *Formal Techniques for Safety-Critical Systems*, pp. 206–222, Springer International Publishing, 2014.

[7] A. Methni, M. Lemerre, B. Ben Hedia, K. Barkaoui, and S. Haddad, "An approach for verifying concurrent c programs," *JRWRTC 2014*, p. 33, 2014.

[8] H. Guesmi, B. Ben Hedia, S. Bliudze, and S. Bensalem, "Externalisation of time-triggered communication system in bip high level models," *JRWRTC 2014*, p. 41, 2014.

[9] A. Methni, M. Lemerre, B. Ben Hedia, S. Haddad, and K. Barkaoui, "C2tla+: A translator from c to tla+," in *TLA+ Community Event*, 2014.

[10] S. Azaiez, B. Ben Hedia, and V. David, "Extracting and verifying viewpoints models in multitask applications," in *VALID*, pp. 64–70, 2011.

[11] L. Morel, J.-P. Babau, and B. Ben Hedia, "Formal modelling framework of data acquisition modules using a synchronous approach for timing analysis," *WRTP/RTS*, vol. 1, 2009.

[12] L. Morel, J.-P. Babau, and B. Ben Hedia, "Towards formal evaluation of qos properties in data acquisition systems using synchronous models," *SYNCHRON'09*, p. 39, 2009.

[13] B. Ben Hedia, F. Jumel, and J.-P. Babau, "Formal evaluation of quality of service for data acquisition systems," in *Proc. of FDL*, vol. 5, 2005.

[14] B. Ben Hedia, F. Jumel, and J. Babau, "Qualite de service des pilotes d'equipements pour les systemes d'acquisition de donnees," *Journal européen des systèmes automatisés*, vol. 39, no. 1/3, p. 47, 2005.

[15] B. Ben Hedia, F. Jumel, and J.-P. Babau, "Evaluation formelle de la qualité de service pour les systèmes d'acquisition," in *RJCITR'05*, p. 23, 2005.

[16] A. Methni, M. Lemerre, B. Ben Hedia, K. Barkaoui, and S. Haddad, "C2tla+: Traduction automatique du code c vers tla," in *ETR'2013*, 2013.

[17] B. Ben Hedia, J. P. BABAU, F. JUMEL, and R. ROBBANA, "Observateurs de propriétés temporelles pour les systèmes d'acquisition de données," in *ETR'07*, 2007.

[18] M. Rabai, B. Ben Hedia, and J.-P. Babau, "Adaptation de l'algorithme jla pour la génération de tâches temps-réel dans un modèle d'exécution time-triggered," in *ETR'13*, 2013.

[19] M. Jan, B. B. Hedia, J. Goossens, and C. Maiza, eds., *22nd International Conference on Real-Time Networks and Systems, RTNS'14, Versaille, France, October 8-10, 2014*, ACM, 2014.

[20] B. B. Hedia and F. P. Vladicescu, eds., *Proceedings of the 9th Workshop on Verification and Evaluation of Computer and Communication Systems, VECoS 2015, Bucharest, Romania, September 10-11, 2015*, vol. 1431 of *CEUR Workshop Proceedings*, CEUR-WS.org, 2015.

[21] B. Ben Hedia, *Analyse temporelle des systèmes d'acquisition de données: une approche à base d'automates temporisés communicants et d'observateurs.* PhD thesis, INSA-LYON, 2008.